

REMARKS

After entry of this amendment, claims 1-24 remain pending. In the present Office Action, the title and claim 10 were objected to. Claims 2-5 and 17-19 were rejected under 35 U.S.C. § 112, first paragraph. Claims 1, 6-8, 13-14, 16, 20 and 22-23 were rejected under 35 U.S.C. § 102(b) as being anticipated by Kahle et al., U.S. Patent No. 5,802,386 ("Kahle"). Claims 1, 13, 15-16, 22, and 24 were rejected under 35 U.S.C. § 102(a) as being anticipated by Hammarlund et al., U.S. Patent Application Publication No. 2003/0126406 ("Hammarlund"). Claims 2-5 and 17-19 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Kahle in view of Markstein et al., U.S. Patent No. 5,631,859 ("Markstein"). Claims 9-10 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Kahle in view of allegedly well known features. Claims 11-12 and 21 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Kahle in view of Hammarlund. Applicants respectfully traverse these rejections and request reconsideration. Additionally, Applicants respectfully traverse the assertion that trace caches are well known (Official Notice of which is taken in the present Office Action). Accordingly, pursuant to MPEP 2144.03, the Examiner is required to provide adequate evidence if the rejection is to be maintained.

Section 112 Rejection

Claims 2-5 and 17-19 were rejected for alleged lack of enablement. Specifically, the Office Action alleges that the predicted precision of operands is not enabled. Applicants respectfully disagree. The specification does enable predicted precision, and using the predicted precision to predict the execution latency. These features are discussed throughout the description of Figs. 2-4. See specifically, for example, specification page 10, lines 2-4; page 10, line 18-page 11, line 7; page 11, lines 9-27; and page 13, lines 13-29. Thus, Applicants respectfully traverse the assertion in the Office Action that the specification is silent on a system that predicts precision and how such precision is predicted.

The Office Action further asserts that operands' precisions are know at the time of execution...there is no prediction requirement to obtain this information. Applicants

agree that the operands precisions are known at the time of execution. However, claim 2 does not recite predicting the precision at the time of execution. At various other times, the precision may be unknown.

Art Rejections

Applicants respectfully submit that each of claims 1-24 recites a combination of features not taught or suggested in the cited art. For example, claim 1 recites a combination of features including: "a prediction circuit configured to predict an execution latency of a floating point operation responsive to a predicted precision of the floating point operation".

With respect to original claim 2, the Office Action asserts that the above highlighted features are obvious in view of Kahle and Markstein. In part, the rejection is based on the Office Action's interpretation of the "predicted precision" as the "predicted precision latency". However, as noted above with regard to the section 112 rejection, the present application's specification does teach predicting the precision, and using the predicted precision to predict the execution latency.

The alleged combination of Kahle and Markstein does not teach or suggest the above highlighted features. Kahle teaches "instruction latency may not always be definitively known, but may be merely predictive. For example, a 'LOAD' instruction may require more than two cycles if there is a cache miss. Predicted instruction latencies are generally sufficient for the purposes of scheduling instructions according to the present invention. It is worth noting, however, that processor cycles identified in the position map are merely predictions of the cycle in which the instruction results are expected to be available." (Kahle, col. 5, lines 24-32) While this section generally discusses predicting instruction latency, it does not teach nor suggest "a prediction circuit configured to predict an execution latency of a floating point operation responsive to a predicted precision of the floating point operation". Markstein teaches a multiplier designed for a given precision, and a microcode routine for performing a higher precision multiplication: "The microcode memory 226 also contains instructions for the quad

precision instructions for divide 226a, square root 226b, multiplication 226c, addition 226d, and subtraction 226e. These quad precision arithmetic instructions are made-up from multiple double-extended instructions and require more than one cycle. The microcode memory 226 also contains instructions for conversion between quad and double double-extended formats 226f, and for quad precision rounding 226g." (Markstein, col. 6, lines 10-18). Accordingly, Markstein teaches a microcode routine that would be called for a quad precision instruction, once the quad-precision operation is detected (i.e. once the precision is known).

For at least the above-stated reasons, Applicants submit that claim 1 is patentable over the cited art. Claims 2-15, being dependent from claim 1, are similarly patentable over the cited art for at least the above stated reasons. Each of claims 2-15 recites additional combinations of features not taught or suggested in the cited art.

Claim 16 recites a combination of features including: " predicting an execution latency of a floating point operation responsive to a predicted precision of the floating point operation". The same teachings highlighted above with regard to claim 1 are alleged to teach the combination of features of claim 16. Applicants respectfully submit that the cited art does not teach or suggest the above highlighted features of claim 16, either. Accordingly, Applicants respectfully submit that claim 16 is patentable over the cited art. Claims 17-24, being dependent from claim 16, are similarly patentable over the cited art for at least the above stated reasons. Each of claims 17-24 recites additional combinations of features not taught or suggested in the cited art.

Claim Objection

Claim 10 was objected to. The Office Action asserts that it is unclear which opcodes are eligible to be selected from, and that Applicants have not disclosed a floating point operation containing more than one opcode. Applicants respectfully submit that claim 10 is clear. Claim 10 recites: "the trace cache is configured to store a selected opcode of at least two opcodes for the floating point operation responsive to the execution latency predicted by the prediction circuit, the selected opcode comprising the

indication of the execution latency". Thus, from the at least two opcodes, a selected opcode is selected for the floating point operation responsive to the predicted execution latency. For example, the specification describes a "fast" opcode and a "slow" opcode (and additional opcodes, in some embodiments). See, e.g., specification page 11, lines 22-27 and page 18, lines 1-2.

Title Objection

The Office Action objected to the title, alleging that the title was not indicative of the claimed invention. Applicants respectfully disagree. However, Applicants have amended the title and respectfully submit that the amended title overcomes the rejection.

Specification Objection

The Office Action Summary indicates that the specification is objected to. However, the only reference to the specification in the body of the Office Action is a general statement that Applicant's cooperation is requested in correcting any errors of which Applicants may be aware. Thus, Applicants respectfully submit that there is no specific objection to the specification.

CONCLUSION

Applicants submit that the application is in condition for allowance, and an early notice to that effect is requested.

If any extensions of time (under 37 C.F.R. § 1.136) are necessary to prevent the above referenced application(s) from becoming abandoned, Applicant(s) hereby petition for such extensions. If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C. Deposit Account No. 501505/5500-91300/LJM.

Also enclosed herewith are the following items:

- ☒ Return Receipt Postcard
- ☐ Petition for Extension of Time
- ☐ Request for Approval of Drawing Changes
- ☐ Notice of Change of Address
- ☐ Fee Authorization Form authorizing a deposit account debit in the amount of \$
for fees ().
- ☐ Other:

Respectfully submitted,



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AGENT FOR APPLICANT(S)

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